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Intel Corporation

Listing of Claims

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method comprising:

receiving an indication that a first peripheral is to participate in an execution of a breakpoint whereas a second peripheral is not to participate;

in response to a first signal indicating ~~the execution of~~ that a processor has encountered ~~a~~ the breakpoint ~~by a processor~~, suspending execution of ~~a~~ the first peripheral and saving the state of the first peripheral;

continuing execution of the breakpoint by the processor and ~~the first peripheral in response to receiving a second signal~~ indicating that the state of the first peripheral has been saved; and

restoring the saved state of the first peripheral in response to a third signal indicating that execution of the breakpoint by the processor has been completed.

2. (Original) The method of claim 1 comprising resuming normal execution of the processor in response to a signal indicating that the saved state has been restored.

3. (Currently Amended) The method of claim 1 comprising resuming normal execution of the first peripheral and the second peripheral in response to a signal indicating that the processor has resumed normal execution.

4. (Currently Amended) The method of claim 1 wherein receiving the indication ~~comprising~~ comprises receiving a setting of a register ~~to control~~ that determines whether generation of the second signal is ~~to be~~ based on the state of the first peripheral.

5. (Currently Amended) The method of claim 1 wherein receiving the indication ~~comprising~~ comprises receiving a setting of a register ~~to control~~ that determines whether generation of a signal indicating that the saved state has been restored is ~~to be~~ based on the state of the first peripheral.

6. (Previously Presented) The method of claim 1 comprising triggering the breakpoint in response to an occurrence of a condition associated with an instruction being executed by the processor.

7. (Currently Amended) A system comprising:

a processor;

a first computer-readable medium storing instructions that, when applied to the processor, cause the processor to:

generate a first signal indicating execution of a breakpoint,

continue execution of the breakpoint in response to receiving a second signal, and

generate a third signal indicating that execution of the breakpoint has been completed;

a first peripheral coupled to the processor;

a second peripheral coupled to the processor;

a second computer-readable medium storing instructions that, when applied to the first peripheral, cause the first peripheral to:

suspend execution and save a state of the first peripheral, in response to receiving the first signal,

continue execution of the breakpoint in response to receiving the second signal, and

restore the state of the first peripheral, in response to receiving the third signal; and

a digital logic circuit comprising a memory that stores an indicator indicating that the first peripheral is to participate in an execution of the breakpoint but the second peripheral is not to participate, wherein

the digital logic circuit is to generate the second signal indicating that the state of the first peripheral has

been saved, and

the digital logic circuit is coupled to the processor, the first peripheral, and the second peripheral.

8. (Currently Amended) The system of claim 7 wherein the first computer-readable medium includes instructions that cause the processor to:

resume normal execution in response to receiving a fourth signal, and

generate a fifth signal indicating that the processor has resumed normal execution; and

wherein the second computer-readable medium includes instructions that cause the first peripheral to resume normal execution, in response to receiving the fifth signal; and

wherein the digital logic circuit is configured to generate the fourth signal indicating that the saved state of the first peripheral has been restored.

9. (Original) The system of claim 8, further comprising:

a second processor;

a third computer-readable medium storing instructions that, when applied to the second processor, cause the second processor to:

suspend execution and save a state of the second processor, in response to receiving the first signal,

restore the state of the second processor, in response to receiving the third signal, and

resume normal execution, in response to receiving the fifth signal; and

the digital logic circuit configured to:

generate the second signal indicating that the state of the second processor has been saved, and

generate the fourth signal indicating that the saved state of the second processor has been restored.

10. (Original) The system of claim 7 including a system on a chip (SOC).

11. (Original) The system of claim 7 including a debugging tool coupled to the system to debug the system.

12. (Currently Amended) The system of claim 7 wherein the ~~digital logic circuit~~ memory comprises a register to ~~control~~ store an indicator of whether generation of the second signal is ~~to be~~ based on the state of the first peripheral.

13. (Currently Amended) The system of claim 7 wherein the state identifies a state of internal registers associated with the first peripheral.

14. (Currently Amended) The system of claim 7 wherein the processor operates at a clock rate different than a clock rate of the first peripheral.

Claims 15.-22. (Canceled)

23. (Currently Amended) An apparatus comprising:

one or more signal lines used to receive signals and to send signals; ~~and~~

a first processor;

a second processor;

a third processor; and

a memory to store an indicator indicating that the second processor is to participate in an execution of a breakpoint but the third processor is not to participate in the execution;

~~a~~ wherein the first processor is configured to:

generate a signal indicating ~~execution of~~ that the first processor has encountered the ~~a~~ breakpoint,

continue execution of the breakpoint in response to receiving a signal on a signal line indicating that the state of a ~~peripheral~~ second processor has been saved, and

generate a signal on a signal line indicating that execution of the breakpoint at the first processor has been completed.

24. (Currently Amended) The apparatus of claim 23 wherein the first processor is configured to resume normal execution in response to a signal indicating that the saved state of the second processor has been restored.

25. (Currently Amended) An apparatus comprising:

one or more signal lines used to receive signals and to send signals; ~~and~~

a first peripheral configured to:

suspend execution and save a state of the first peripheral[[,]] in response to receiving a signal indicating ~~execution of~~ a breakpoint has been encountered, and

restore the state of the first peripheral, in response to receiving a signal indicating that execution of the breakpoint has been completed;

a second peripheral configured to suspend execution in response to receiving the signal indicating the breakpoint has been encountered; and

a memory to store an indicator indicating that the first peripheral is to participate in the execution of the breakpoint but the second peripheral is not to participate in the execution.

26. (Currently Amended) The apparatus of claim 25 wherein the second peripheral is configured to resume normal execution

in response to a signal indicating that a processor has resumed normal execution.

27. (Currently Amended) The method of claim 1 wherein saving the state of the first peripheral comprises saving the state of an input/output device.

28. (Previously Presented) The method of claim 27 wherein saving the state of the input/output device comprises saving the state of a universal asynchronous receiver/transmitter (UART).

29. (Currently Amended) The method of claim 1 wherein suspending execution of the first peripheral comprises suspending execution of a peripheral that is monolithically fabricated on a same chip as the processor.

30. (Currently Amended) The system of claim 7 wherein the first peripheral comprises an input/output device.

31. (Previously Presented) The system of claim 30 wherein the input/output device comprises a universal asynchronous receiver/transmitter (UART).

32. (Currently Amended) The system of claim 7 wherein the system comprises a monolithically fabricated chip that includes the processor, the first peripheral, and the second peripheral.

Claim 33.-38. (Canceled)

39. (Currently Amended) The apparatus of claim 23 wherein the apparatus comprises a monolithically fabricated chip that includes the first processor, the second processor, and the ~~peripheral~~ third processor.

40. (Currently Amended) The system of claim 25 wherein the first peripheral comprises an input/output device.

41. (Previously Presented) The system of claim 40 wherein the input/output device comprises a universal asynchronous receiver/transmitter (UART).

42. (Currently Amended) The apparatus of claim [[26]] 25 wherein the apparatus comprises a monolithically fabricated chip that includes the processor, the first peripheral, and the second peripheral.